



STP5NK65Z

N-CHANNEL 650V - 1.5Ω - 5A TO-220
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP5NK65Z	650 V	< 1.8 Ω	5 A	85 W

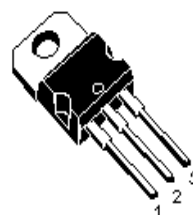
- TYPICAL R_{DS(on)} = 1.5 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

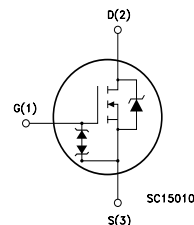
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC



TO-220

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP5NK65Z	P5NK65Z	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	650	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	650	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	5	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	3.1	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	20	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	85	W
	Derating Factor	0.6	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	2000	V
$dv/dt (1)$	Peak Diode Recovery voltage slope	4.5	V/ns
T_j	Operating Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage Temperature	-55 to 150	$^\circ\text{C}$

($\bullet$) Pulse width limited by safe operating area

(1) $I_{SD} \leq 5\text{A}$, $di/dt \leq 100 \mu\text{A}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case Max	1.64	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	50	$^\circ\text{C/W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	4.2	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	190	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED)
 ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.1 \text{ A}$		1.5	1.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 2.1 \text{ A}$		5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		680 80 17		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 480 \text{ V}$		98		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 325 \text{ V}$, $I_D = 2.1 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		20 15		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 520\text{V}$, $I_D = 4.2 \text{ A}$, $V_{GS} = 10\text{V}$		25 4.4 13.7	35	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 325 \text{ V}$, $I_D = 2.1 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		140 40		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 520 \text{ V}$, $I_D = 4.2 \text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		12 7 15		ns ns ns

SOURCE DRAIN DIODE

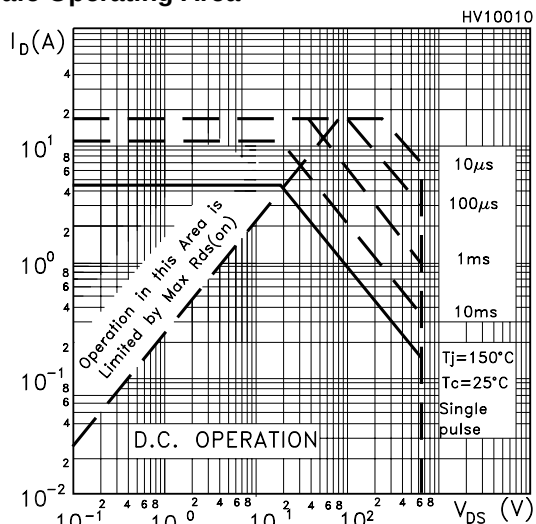
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				5 20	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 5 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4.2 \text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 100\text{V}$, $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		375 1.76 10		ns μC A

 Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

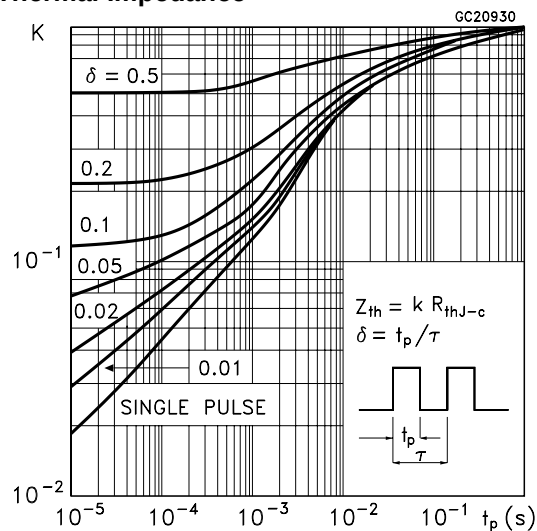
2. Pulse width limited by safe operating area.

 3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

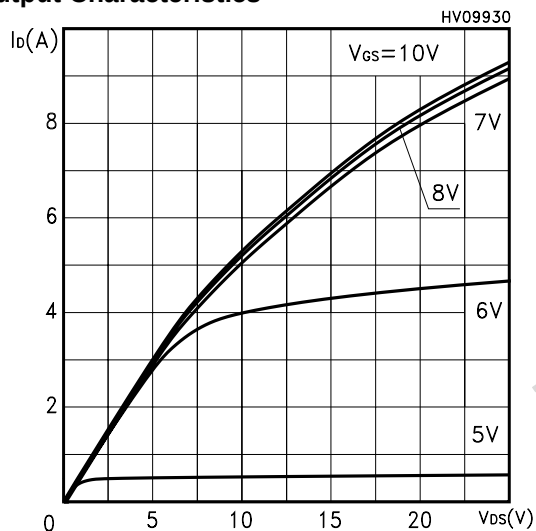
Safe Operating Area



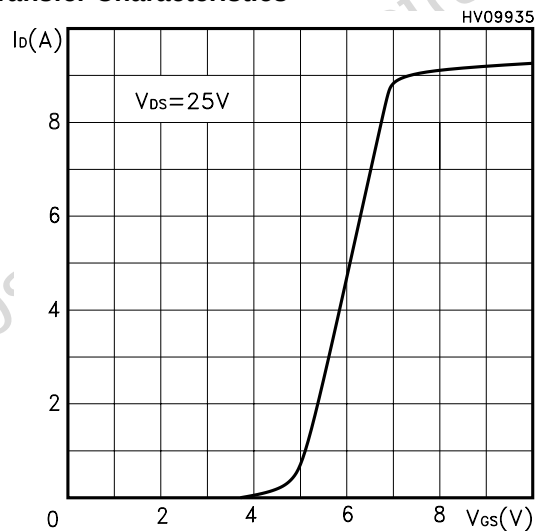
Thermal Impedance



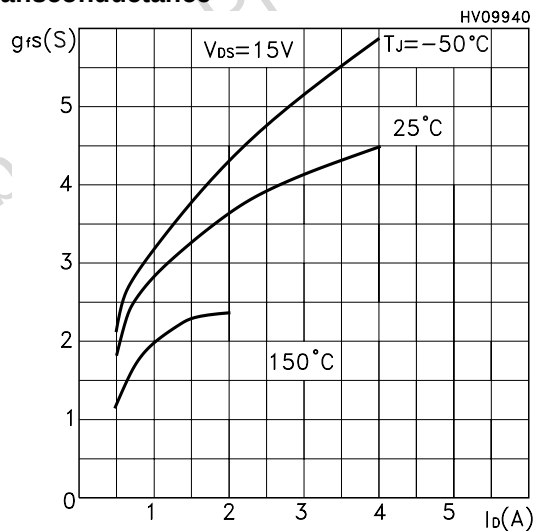
Output Characteristics



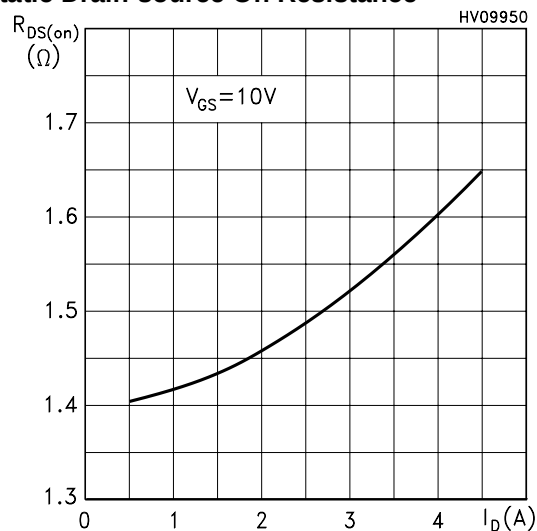
Transfer Characteristics



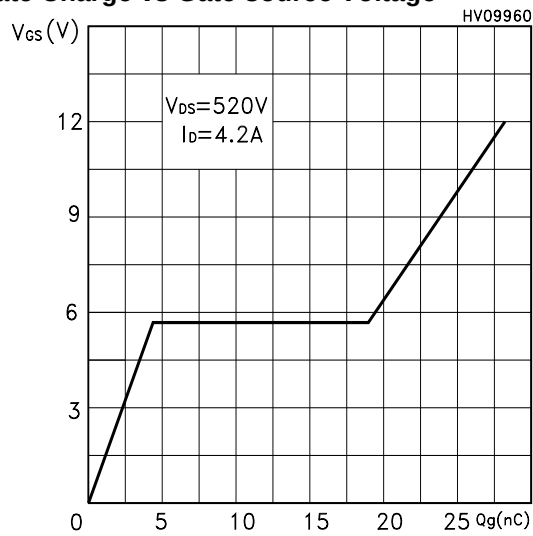
Transconductance



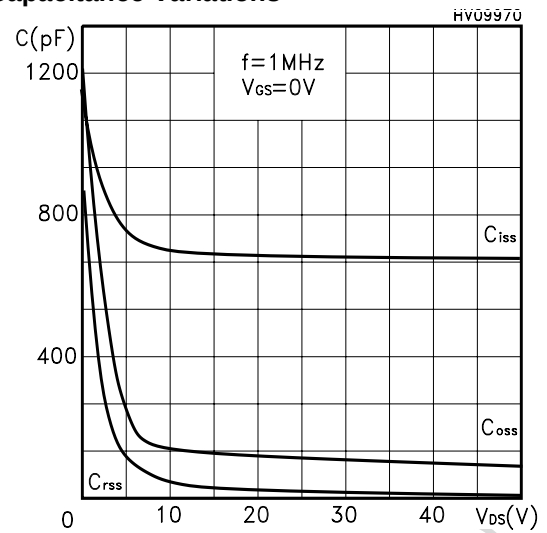
Static Drain-source On Resistance



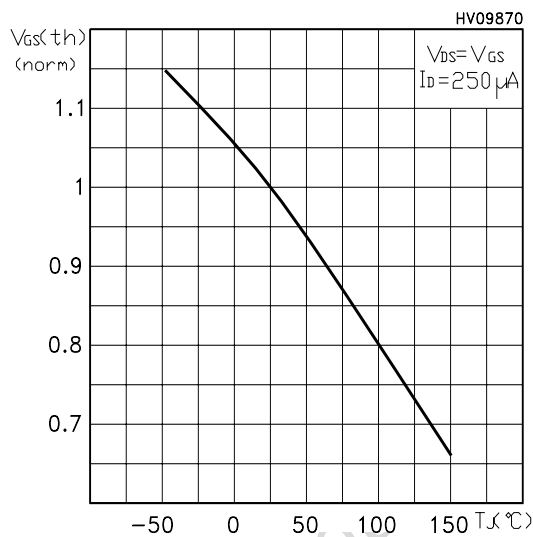
Gate Charge vs Gate-source Voltage



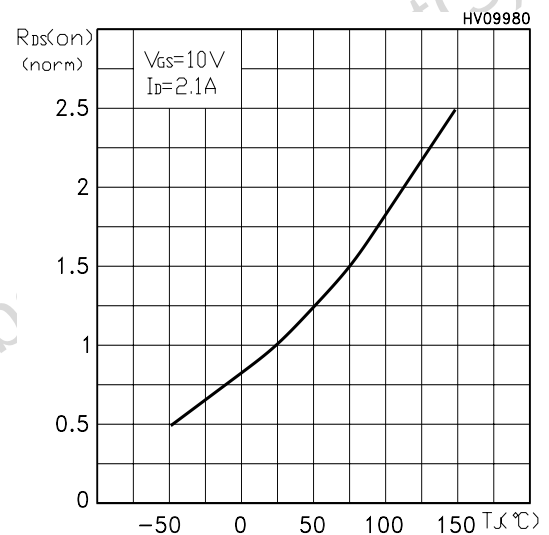
Capacitance Variations



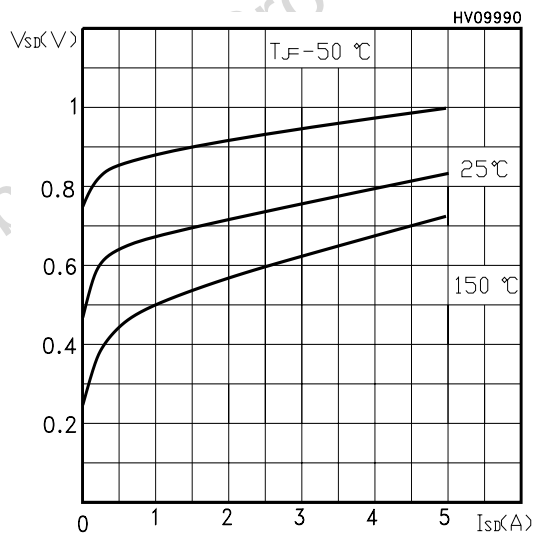
Normalized Gate Threshold Voltage vs Temp.



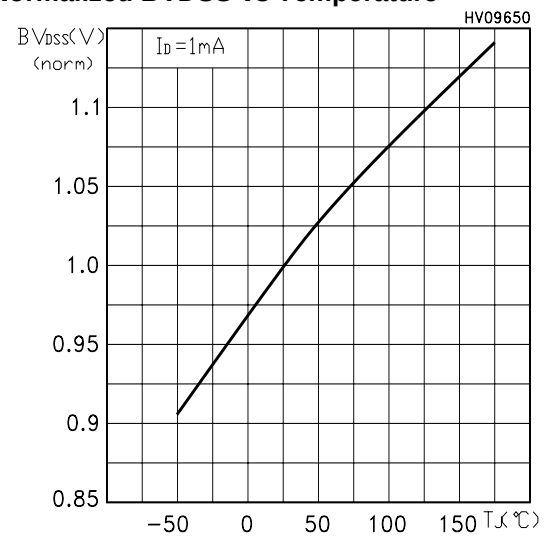
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

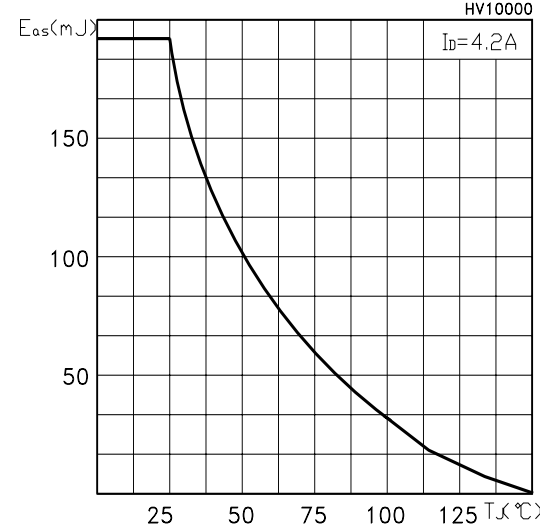
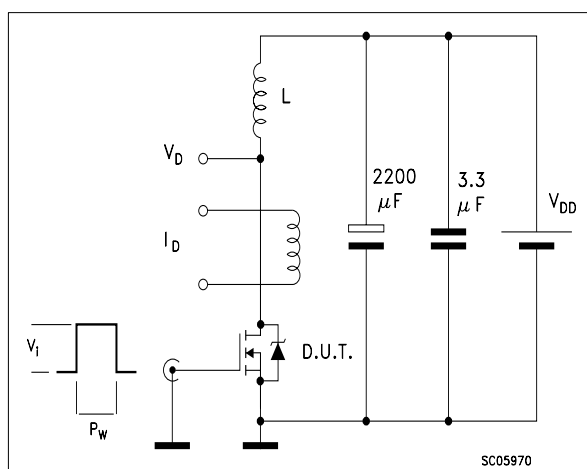
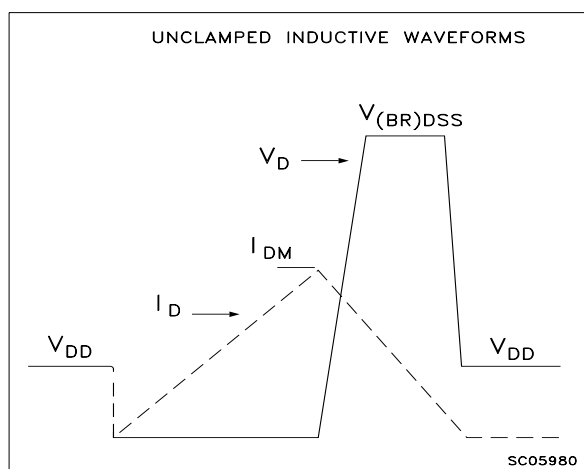
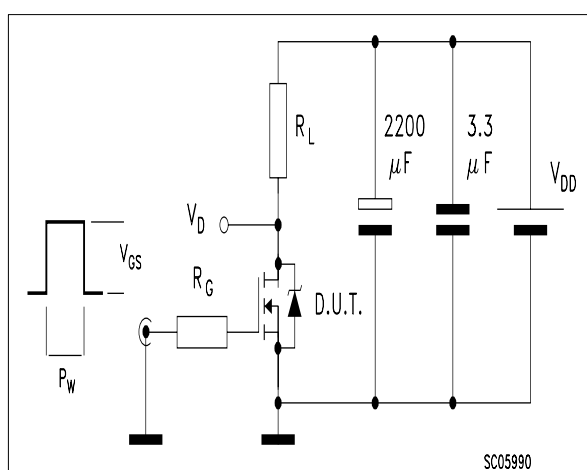
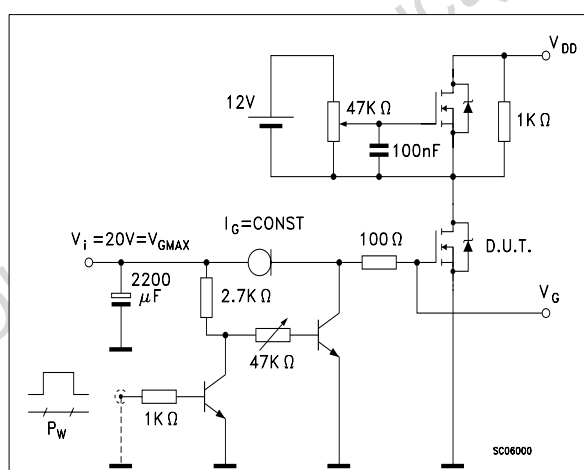
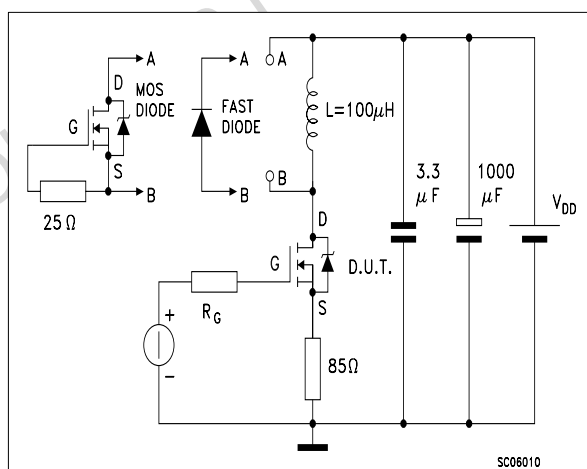
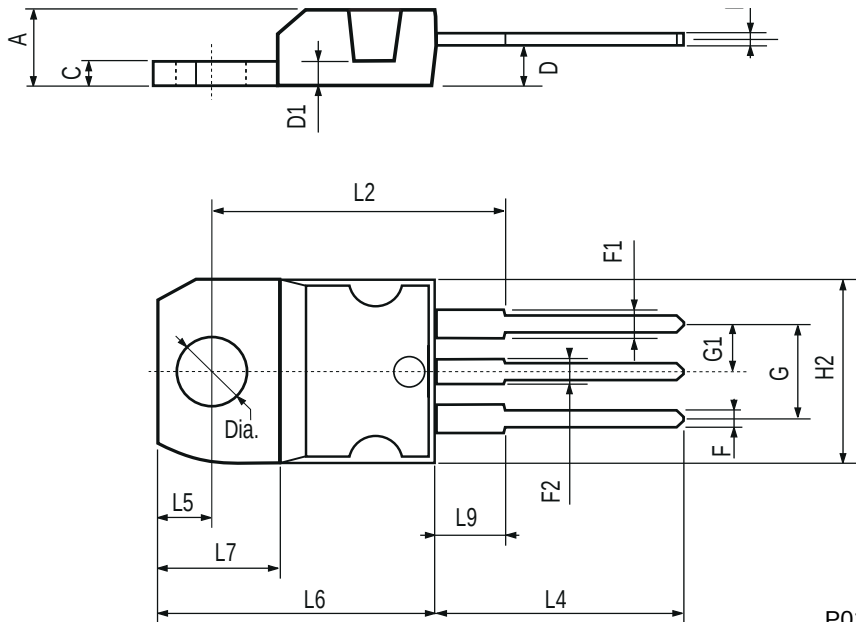


Fig. 1: Unclamped Inductive Load Test Circuit**Fig. 2: Unclamped Inductive Waveform****Fig. 3: Switching Times Test Circuit For Resistive Load****Fig. 4: Gate Charge test Circuit****Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**

TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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